Silicon capacitors: a new solution for decoupling applications

By Laetitia Omnès

As consumers are eager to get the most cutting-edge products, manufacturers have to adapt their technologies and continue to drive innovations to offer the most advanced electronic equipment. Two key features must often be considered for electronic devices: size and performance. In order to anticipate the demand for more miniaturization and signal integrity over a wide range of frequencies in the decoupling applications, IPDIA adds to its silicon passive component library some ultra low ESR/ESL structures, in low profile form factor. These new silicon capacitors enable to drastically decrease the overall impedance and offer the best solution for decoupling performances up to 10 GHz frequency range.

In the case of embedded applications and System in Package modules, not only must the size of the device be optimized in x and y axes, the thickness is also highly important. IPDIA provides a full range of silicon capacitors, including some with ultra-low profile - down to 30 μm - developed and offered for decoupling applications with space constraints.

In terms of performance for decoupling applications, the main feature that needs to be improved is the signal integrity of the integrated circuit. On top of the low profile feature, these applica-

tions are very demanding in signal integrity and decoupling capacitors are considered to be one of the best solutions in terms of efficiency and cost to reduce the voltage fluctuation. However, decoupling capacitors are not perfect and their performance depends not only on the capacitance but also on the Equivalent Series Resistance (ESR) and on the Equivalent Series Inductance (ESL).

The total ESR is the sum of the resistance of the dielectric material (frequency dependent) and the resistance of the conductive parts (constant value). For a long time, ESR was the main parameter to be considered. But as the race for higher-speed applications gathers pace, capacitors with low impedance at higher frequencies are needed. This trend leads manufacturers and designers to take into account the ESL parameter. This further complicates the work of designers, who need to consider the constraints imposed by these parameters. The IPDIA R&D team has addressed this issue with its high density capacitors.

Ultra low profile silicon capacitors

The manufacture of IPDIA passive components is based on the PICS (Passive Integration Connecting Substrate) developed in IPDIA’s own R&D center. This technology takes advantage of the thickness of silicon to integrate hundreds of passive components such as high-Q inductors, resistors, MIM capacitors and trench MOS capacitors in one single die. This technology has already proved its efficiency in terms of area saving. The 3D trench depth of the silicon capacitor drives the results obtained in terms of thickness and capacitor density. Table 1 shows the die thickness obtained and the corresponding capacitor density, figure 1 shows a 100 μm die embedded in a PCB.

On top of the low profile specifity, these 3D silicon capacitors, already in mass production, offer a capacitance density up to 260 nF/mm² with a breakdown voltage (VBD) of 11V minimum.

Their “Intrinsic lifetime” to 0.1% is over 10 years at 3.6V, 100°C (60% C.I.) even for corner batches.

The devices have low leakage (typically < 5 nAμF) and down to < 0.2 nAμF at 3.2V/25°C), and a high capacitance stability with respect to temperature (70 ppm/°C over the -55°C/+200°C range) or voltage (<0.1%/V).

ESR/ESL contribution

To cope with the increased demand for more sensitive devices and faster transition in the IC, power integrity must be guaranteed and therefore impedance minimized while maintaining the availability of a wide range of capacitance values. The output ripple voltage is directly related to ESR values. As input/output voltages of modern DC/DC converters are getting lower and lower, this input/output ripple due to ESL is an increasingly important parameter that has become challenging to solve with standard MLCCs. In the past decades, all capacitor parameters were measured at a standard of 1MHz, as DCDC converters were operating at 10MHz. But in today’s high frequency world where the trend in DC/DC converters is to operate in ranges of tens of MHz, this is far from sufficient. Ideal values for a good high frequency capacitor for a given capacitance could run in the order of about

Laetitia Omnès is responsible for Marketing and Communications at IPDIA – www.ipdia.com – She can be reached at laetitia.omnes@ipdia.com

Fig. 1: 100 μm die embedded in a PCB.

Fig. 2: Standard PICS capacitor design compared with Mosaic PICS capacitor design. The ESR is driven by the capacitor shape/outer extend in the standard design when it depends on the localized element in the Mosaic. ESL/Global becomes a variation of 1/N in the second case, N being the number of elementary cells parallelized.
50 mΩ at 200 MHz, 110 mΩ at 900 MHz and 140 mΩ at 2 GHz. To reach a global impedance of 140 mΩ at 2 GHz, as this frequency is way above the SRF, several MLCCs must be added in parallel. Designers, however, need to find a capacitor with very low impedance over a broad frequency range.

IPDIA R&D’s team of expert has addressed this issue and has set up a new PICS capacitor quasi fractal design, so called ‘Mosaic’ that provides a way to reduce the ESR/ESL of the global structure – see figure 2. The approach consists in increasing the contact density with the electrode to obtain a less resistive backend (metallic) grid. Optimization is carried out to minimize the grid ESR and ESL while the individual Mosaic cells are massively parallelized to control the global ESR/ESL.

When comparing this new generation of silicon capacitors with X7R and COG 100 nF capacitors – see figure 3 – we can see that no inductive transition is observed up to 10 GHz for the PICS capacitor and that it acts as a low-impedance element over a wide range of frequencies while X7R and COG capacitors act as low-impedance elements over a limited range of frequencies. IPDIA PICS capacitor provides the best result in terms of low impedance for frequencies higher than 20 MHz compared with COG and 35 MHz compared with X7R.

Comparing capacitance density, we observed that whilst offering 100 times more capacitance density (2000 nF/mm³ vs 20 nF/mm²), IPDIA 3D Silicon capacitors also offer better ESR characteristics (20 mΩ versus 100 mΩ when compared with Type I capacitors). For Type II, IPDIA offers unique capacitance stability performance with an ultra-low profile of 80 µm and 20mΩ of ESR when X7R and X5R capacitors offer a standard thickness of 300 µm at the same level of ESR, with lower stability performance.

Improving decoupling performance has usually been based on the idea of reducing the ESR. Low ESR MLCCs have been widely used for this purpose. However, nowadays, in new DC/DC converters operating at much higher frequencies, a very low impedance device is required. A standard capacitor can in fact only be used up to the SRF. Above the SRF, the user essentially has a “DC blocking inductor”. In order to extend the usable frequency range in such applications, IPDIA is offering ultra low ESL structures, in a low profile form factor, which drastically decrease the overall impedance above the SRF and offer the best solution for decoupling performances in the 35 MHz to 10GHz frequency range.

<table>
<thead>
<tr>
<th>Process Node</th>
<th>Capacitor Density</th>
<th>Minimum die thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>PICS1</td>
<td>25 nF/mm²</td>
<td>30 µm</td>
</tr>
<tr>
<td>PICS2</td>
<td>80 nF/mm²</td>
<td>50 µm</td>
</tr>
<tr>
<td>PICS3</td>
<td>250 nF/mm²</td>
<td>80 µm</td>
</tr>
</tbody>
</table>

Table 1: Die thickness and the corresponding capacitor density.

Fig. 3: Impedance magnitude for 100 nF capacitor element. Comparison of PICS, COG and X7R.

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Understanding the distortion mechanism of high-K MLCCs

By John Caldwell

THE UNDERLYING MECHANISM causing distortion when using High-K ceramic capacitors in a system’s signal path is the voltage coefficient of capacitance (VCC) of the capacitor.

The term VCC is used to describe the change in the value of a capacitor with respect to the magnitude of the applied voltage. Power supply designers are well aware of this behaviour as it can directly affect the output ripple or stability of their system, but VCC is often ignored in small-signal circuitry. In order to understand why the capacitance varies with applied voltage and how the VCC varies with other capacitor parameters, it is necessary to first look at a capacitor’s basic structure.

Figure 1 shows a simple capacitor consisting of two plate electrodes of area A, separated a distance d by a dielectric (green). The capacitance of this structure is given by equation 1:

\[ C = \frac{\varepsilon_r \varepsilon_0 A}{d} \]

where \( \varepsilon_0 \) and \( \varepsilon_r \) are the permittivity of free space and relative permittivity of the dielectric, respectively. The magnitude of the electric field applied to the dielectric is a function of the applied voltage and the separation distance between the two plates.

\[ |E| = \frac{V}{d} \]

The voltage coefficient of many capacitors arises from the electrostatic force on the dielectric when a voltage is applied to the capacitor.

\[ F = \frac{\varepsilon_0 \varepsilon_r AV^2}{2d^2} \]

Because the dielectric material cannot be infinitely stiff, it is compressed by this force, reducing the separation distance d and increasing the capacitance. Multilayer ceramic capacitors, on the other hand, exhibit an additional negative voltage coefficient that arises from other properties of the dielectric.

Ceramic capacitors owe their small size, high capacitance, and low cost to the use of barium titanate in the dielectric, which provides an extremely high relative permittivity. Unfortunately, this material’s relative permittivity varies depending upon the intensity of the applied electric field – see figure 2. As the applied electric field is increased, the relative permittivity of the barium titanate is reduced, showing a 55% reduction over the tested range. Therefore, increasing the voltage applied to a ceramic capacitor reduces the relative permittivity of the barium titanate in the dielectric material, causing a decrease in capacitance.

The electric field intensities in figure 2 may seem unlikely to occur in small signal circuits. However, in the pursuit of higher volumetric efficiencies, capacitor manufacturers are able to produce ceramic capacitors with dielectric thicknesses below 5 microns, creating surprisingly high electric field intensities. Using equation 2, we can see that applying 1V to a capacitor with a 5 μm dielectric thickness results in an electric field intensity of 200,000 V/m.

Understanding this property of barium titanate allows us to infer some rules for the voltage coefficient of ceramic capacitors. First, the voltage coefficient is worst (greatest change with applied voltage) in ceramic capacitors with the highest barium titanate content. Table 1 displays the barium titanate content of selected ceramic dielectric types.

Second, the voltage coefficient gets worse for smaller packages because the change in the relative permittivity is dependent upon the intensity of the applied electric field. As the capacitor’s package size is decreased, the area of the electrode plates is reduced. Therefore, the thickness of the dielectric must be reduced to maintain a certain capacitance.

**Voltage coefficient effects**

Although we’ve identified the mechanism for voltage coefficient of capacitance, it may not be immediately clear how this voltage coefficient causes distortion. Consider that because the value of a ceramic capacitor is, in reality, a function of the applied voltage, the equation for current through that capacitor must be modified. As shown in the equation below, the constant C for capacitance is replaced with a function C, which depends on the applied voltage \( V \).

\[ i = C(V) \cdot \frac{dV}{dt} \]

We can extract the function \( C(V) \) from typical voltage coef-
Table 1: Barium titanate content of selected ceramic capacitor dielectric types [4]

<table>
<thead>
<tr>
<th>Dielectric Type</th>
<th>Barium Titanate Content</th>
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<tbody>
<tr>
<td>COG</td>
<td>10% to 50%</td>
</tr>
<tr>
<td>X7R</td>
<td>90% to 98%</td>
</tr>
<tr>
<td>ZSU</td>
<td>80 to 94%</td>
</tr>
<tr>
<td>Z5V</td>
<td>80 to 94%</td>
</tr>
</tbody>
</table>

In the previous example, a 50 Vpk sine wave was chosen such that the distortion of the current waveform would be visibly noticeable. However, these effects begin at much lower voltages.

**Simulating with non-ideal capacitors**

The effect on the current waveform may seem miniscule, but the degree to which it degrades the total harmonic distortion of a circuit can be surprising. In order to prove this, a SPICE model for a polynomial non-linear capacitor (polycap) was modified to incorporate the cubic equation for voltage coefficient, C(V). This model approximates a nonlinear capacitor using a controlled current source whose output current is defined by the polynomial equation for C(V), as well as the derivative of the applied voltage with respect to time, dV/dt. The time derivative is determined by applying a copy of the applied voltage across a known capacitance CREF, and measuring the resulting current.

The model accepts four parameters: C0, C1, C2, and C3. These can be positive or negative and define the capacitor's voltage coefficient equation.

Figure 4 shows the predicted effect of an applied 50 Vpk, 1 kHz sine wave on the capacitance of a 10 nF, 50V X7R capacitor. The capacitance value dips over the period of the sine wave, reaching a minimum of 8.56 nF at the maximum applied voltage of 50V.

The effect of the voltage coefficient on the current waveform in the capacitor can be produced by inserting into equation 4 the cubic equation for C(V) extracted in figure 3. Figure 5 compares the ideal current waveform of a 10 nF capacitor for a 50 Vpk, 1 kHz sine wave to the actual waveform when including the effects of the voltage coefficient. The voltage coefficient distorts the current waveform into a more triangular shape, indicating the introduction of odd harmonics into the signal path.

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Fig. 4: The predicted instantaneous change in capacitance of a 10 nF, 50V, X7R capacitor resulting from an applied 40Vp sine wave.

Fig. 5: Ideal and actual current through a capacitor considering voltage coefficient effects

Because the cubic equation for C(V) extracted in figure 3 is only defined for voltages greater than zero, the absolute value function must be incorporated to accurately model the capacitance value for both positive and negative voltages. This approach was found to be much more accurate than attempting to fit a polynomial over the entire range of possible voltages (both positive and negative). A Sallen-Key 1 kHz lowpass filter was simulated using polynomial nonlinear capacitor models for 10 nF and 22 nF, 50V X7R capacitors. Figure 7 shows the simulation schematic incorporating X7R capacitors CX1 and CX2.

TINA was used to perform a Fourier Spectrum analysis of the output of the filter for a 500 Hz, 1 Vrms input signal. A 65536-sample FFT was performed on an 80 ms sample of the output signal to produce the spectrum. In order to avoid the use of windowing, the time steps of the simulation were constrained and the input signal was chosen to be a coherent frequency.

Fig. 7: Simulation schematic of a Sallen-Key 1 kHz lowpass filter with X7R capacitors shown as CX1 and CX2.

Fig. 8: TINA Fourier spectrum analysis of a 500 Hz sine wave applied to the filter circuit using nonlinear capacitor models (top) and ideal capacitor models (bottom).

Any harmonics in the output spectrum are the result of the capacitors' voltage coefficient because the distortion characteristic of the operational amplifier (op amp) is not modelled below the full power bandwidth limitation.

Figure 8 shows the simulated output spectrum of the circuit when using the modeled X7R capacitors (blue) compared to idealized capacitors (red). The simulation shows a large number of predominantly odd order harmonics are produced when using X7R capacitors in the filter circuit, which agrees with the results from the first article.

As expected, the simulation using ideal capacitors shows only a spur at the fundamental frequency. The amplitude of the harmonics in the simulation, on average, is 10 dB lower than that measured in the actual circuit (using capacitors with more pronounced voltage coefficients than those chosen for the simulation model).

Conclusion

In ceramic capacitors, the relative permittivity of the dielectric is changed by the intensity of the applied electric field, giving rise to a substantial voltage coefficient. This effect is worst in high-K dielectric types and smaller package sizes. As a result, the value of the capacitor is changing instantaneously due to the applied signal, causing distortion in the current waveform. We demonstrated this by producing a SPICE model for a capacitor that replicates the voltage coefficient of a typical 50V X7R capacitor. The X7R capacitor models produced a large number of harmonics when used to simulate a Sallen-Key lowpass filter. In wide dynamic range applications where a substantial voltage may appear across a capacitor, it is best to select C0G, polypropylene film, or silvered mica capacitors to avoid excess distortion.
Additive photolithographic process yields micro flex circuits with 5µm feature resolution

Using additive photolithographic processes, Metrigraphics is able to manufacture Extreme Resolution Micro Flex (ERMF) ultra-miniature passive circuits and structures with traces and spaces as small as 5µm. The circuits can also be delivered in complex, high-resolution shapes and patterns for medical sensor applications, including various in body and fluid sensors. The micro circuits are produced with very thin layers of sputtered metal or thicker plated metal such as gold or copper. The company reports that its processes can achieve traces as narrow as 3µm for some designs. Metrigraphics offers both single and multilayer ERMF circuits. Multilayer circuits include additional conductive layers that are independently stacked, aligned and interconnected. Plated conductive vias connect the different layers as required. Via sizes can be down to 25µm diameter.

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API Delevan now offers three SMD power inductors with the highest reliability rating available after achieving a "T" Level reliability rating. The MILP1812, MIL4922 and MIL8532 meet all Military QPL requirements, and the ruggedized moulded and leaded construction is proven against MIL-STD-202 mechanical vibration, moisture resistance, and DWV testing. All "T" Level inductors are thermally shocked for 25 cycles, burn-in for 96 hours, and x-ray inspected before customer delivery. High-saturation ferrite core materials and thick AWG size wire offer these inductors higher operating power along with maximum operating efficiency, resulting in a cooler running product.

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Automotive-qualified passives

Murata has extended its automotive qualified MLCC offering with addition of AEC-Q200 and ISO7637-2 parts. Added to Murata’s AEC-Q200 qualified multi layer ceramic capacitors (MLCC) aimed at automotive applications are the RCE and RHE series radial leaded MLCCs that fully conform to the automotive environmental stress test requirement AEC-Q200 and conducted surge pulse immunity specification ISO7637-2. The RCE series comprises capacitors in the range 1 pF to 22 µF and working voltage from 25 to 1 kV. Operating temperature range is up to 125°C. With an operating temperature up to 150°C the RHE series devices are available with 50 to 100 VDC working voltage and capacitance values from 100 pf to 10 µF. The RHE series is guaranteed to operate in temperatures up to 170°C for 100 hours when a temperature mission profile is agreed with Murata in advance.

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TDK further shrinks common-mode chokes for CAN and FlexRay

For deployment in both CAN and FlexRay data bus environments, TDK has developed the ACT1210 series of common-mode chokes. Measuring only 3.2x2.5x2.4mm, the chokes are the world’s smallest, claims TDK, taking 45% less PCB space than that of existing components. Rated for a wide operating temperature range from -65 to +150°C, the ACT1210 series offers high heat resistance and reliability, making it suitable for use under severe conditions such as those encountered in the engine compartment of a vehicle. The ACT1210 common-mode chokes employ an improved ferrite and is based on the joint technology competence of TDK and EPCOS in the area of EMC. Thanks to the structural design of the new series, the components are manufactured using a high-precision autowinding process.

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The RHC2512 from Stackpole is a high power 2W-rated 2512 size chip resistor claimed to have a much lower heat rise compared to other high power chip resistors currently available. Stackpole uses a unique set of materials, part design, and manufacturing processes to lower the self-heating of the part by at least 30 degrees C. The RHC2512 is available in values from 0.1 Ohms up to 1M Ohm in 1% and 5% tolerances and TCR of 100 ppm. The RHC Series can be used in a wide range of applications, including professional, commercial, and industrial power systems; control systems; and industrial and commercial automation.

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